UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/758,494	01/15/2004	John Rha	0150140	6169

25700 7590 06/24/2005

FARJAMI & FARJAMI LLP
26522 LA ALAMEDA AVENUE, SUITE 360
MISSION VIEJO, CA 92691

EXAMINER	
COLEMAN, WILLIAM D	
ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 06/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/758,494	RHA ET AL.	
	Examiner	Art Unit	
	W. David Coleman	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Objections

1. The terms "ESC" and "VRF" are not disclosed reasonably enough to provide one with ordinary skill in the art with a generally accepted acronym or meaning. Please note that the terms "ESC" and "VRF" are not enforceable if the Applicants ever becomes a patent. Correction is required.

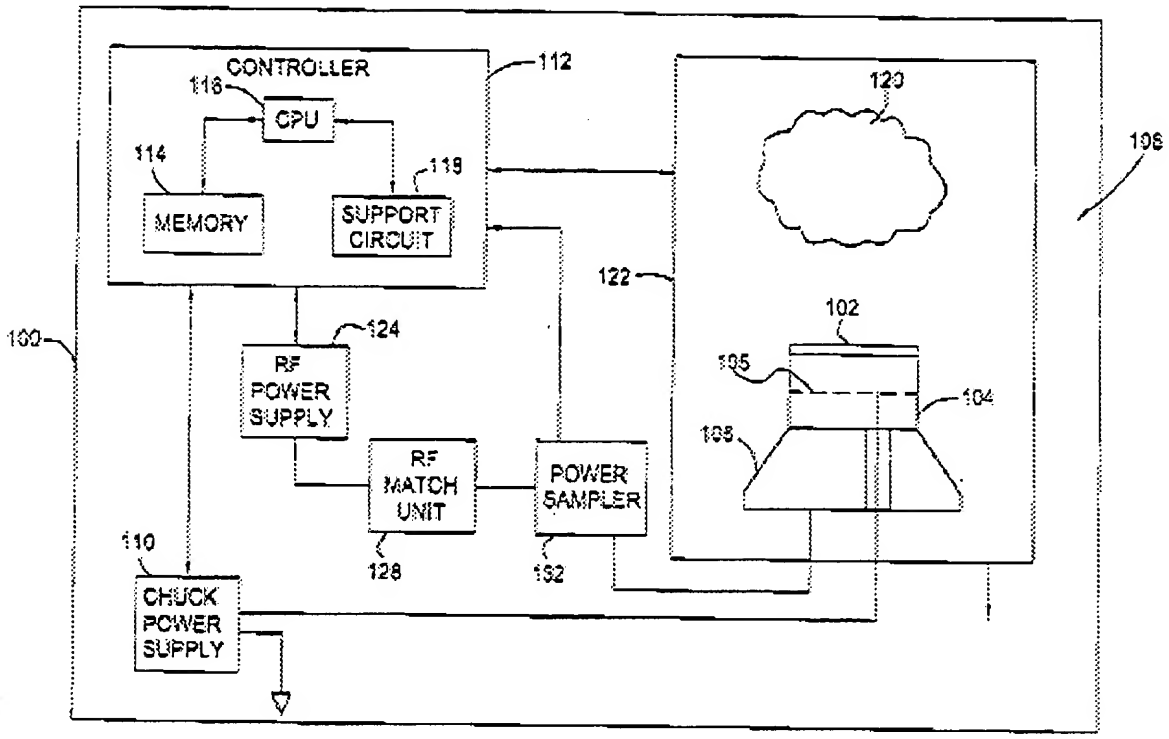
Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Shoji discloses a circuit substantially as claimed. Please see FIGS. 1-8 where Shoji teaches the following limitations.

4. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shoji U.S. Patent Application Publication No. U.S. 2004/0031699 A1 in view of Johnson, Jr. et al., U.S. Patent 5,175,472.



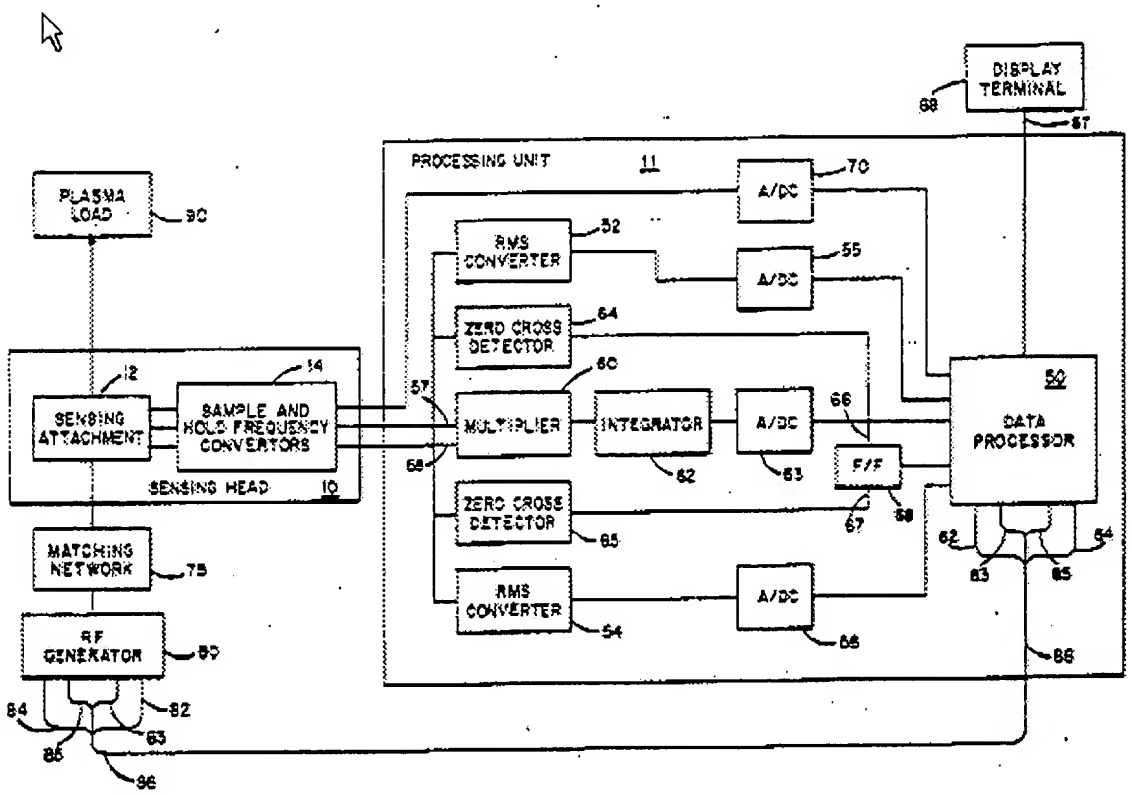
5. Pertaining to claim 1, Shoji teaches a circuit configured to interface with an etch tool, said circuit comprising:

an ESC input for receiving a first signal **132** from said etch tool (the etch tool in this case is the chuck **104**), said first signal indicating a magnitude of a chuck current passing through a chuck holding a wafer in said etch tool;

a VRF input for receiving a second signal from said etch tool, said second signal indicating a magnitude of a voltage difference between a plasma and said chuck in said etch tool;

an arc detect output **112** indicating whether an arc event has occurred. However, Shoji does not specifically use the term "VRF input" for receiving a second signal from said etch tool. The Examiner takes the position that the VRF is equivalent to either the Sample and Hold Frequency converter **14** of Johnson or the A/DC 70, 55, 63 or 56.

See Johnson **FIG. 1**. In view of Johnson, it would have been obvious to one of ordinary skill in the art to incorporate the input receiving circuit into the Shoji circuit because RF power source can be maintained irrespective of impedance fluctuations (see Abstract).



6. Pertaining to claim 2, Shoji in view of Johnson teaches the circuit of claim 1 wherein said circuit is configured to prevent said arc detect output from indicating an occurrence of a chucking spike and a de-chucking spike in said etch tool.

7. Pertaining to claim 3, Shoji in view of Johnson teaches the circuit of claim 1 wherein said first signal indicates an occurrence of the group consisting of a chucking spike, a de-chucking spike, and said arc event in said etch tool.

8. Pertaining to claim 4, Shoji in view of Johnson teaches the circuit of claim 1 further comprising an ESC signal level detector connected to said ESC input, said ESC signal level detector being configured to provide an output when said first signal indicates an occurrence of the group consisting of a chucking spike, a de-chucking spike, and said arc event.

9. Pertaining to claim 5, Shoji in view of Johnson teaches the circuit of claim I further comprising a VRF signal level detector connected to said VRF input, said VRF signal level detector being configured to provide an output when said second signal indicates that said plasma is activated.

10. Pertaining to claim 6, Shoji in view of Johnson teaches the circuit of claim 1 further comprising a first gate having a first gate input, a second gate input, and a first gate output, said first gate input being connected to said ESC input and said second gate input being connected to said VRF input, said first gate being configured to output a third signal at said first gate output when said first signal indicates an occurrence of a de-chucking spike and said arc event and not output said third signal at said first gate output when said first signal indicates an occurrence of a chucking spike (the Examiner takes the position that since there are at least 3 A/DC converters there are at least 3 signals).

11. Pertaining to claim 7, Shoji in view of Johnson teaches the circuit of claim 6 further comprising a power-on delay connected between said VRF input and said second gate input, said power-on delay being configured to prevent said first gate from outputting said third signal

during said occurrence of said chucking spike (the Examiner takes the position that it is well known that A/DC converters have more that one gate electrode).

12. Pertaining to claim 8, Shoji in view of Johnson teaches the circuit of claim 6 further comprising a second gate having a third gate input, a fourth gate input, and a second gate output, said third gate input being connected to said first gate output and said fourth gate input being connected to said VRF input, said second gate being configured to output a fourth signal at said second gate output during said occurrence of said arc event and not output said fourth signal at said second gate output during said occurrence of said de-chucking spike (please see the explanation in the rejection of claim 7 above).

13. Pertaining to claim 9, Shoji in view of Johnson teaches the circuit of claim 1 further comprising a storage module having an input and an output, said output of said storage module being connected to said arc detect output, said storage module being configured to store a third signal received at said input of said storage module and output said third signal at said output of said storage module, said third signal indicating an occurrence of said arc event.

14. Pertaining to claim 10, Shoji in view of Johnson teaches the circuit of claim 6 further comprising a power-off advance connected to said first gate output, said power-off advance being configured to prevent said arc detect output from indicating said occurrence of said de-chucking spike (see **FIG. 3** of Shoji).

15. Pertaining to claim 11, Shoji in view of Johnson teaches a circuit configured to interface with an etch tool, said circuit comprising:

an ESC input for receiving a first signal from said etch tool, said first signal indicating a magnitude of a chuck current passing through a chuck holding a wafer in said etch tool;

a VRF input for receiving a second signal from said etch tool, said second signal indicating a magnitude of a voltage difference between a plasma and said chuck in said etch tool;

an arc detect output indicating whether an arc event has occurred; wherein said circuit is configured to prevent said arc detect output from indicating

an occurrence of a chucking spike and a de-chucking spike in said etch tool. However, Shoji does not specifically use the term "VRF input" for receiving a second signal from said etch tool. The Examiner takes the position that the VRF is equivalent to either the Sample and Hold Frequency converter **14** of Johnson or the A/DC 70, 55, 63 or 56.

See Johnson **FIG. 1**. In view of Johnson, it would have been obvious to one of ordinary skill in the art to incorporate the input receiving circuit into the Shoji circuit because RF power source can be maintained irrespective of impedance fluctuations (see Abstract).

16. Pertaining to claim 12, Shoji in view of Johnson teaches the circuit of claim 11 wherein said first signal indicates an occurrence of the group consisting of said chucking spike, said de-chucking spike, and said arc event in said etch tool.

17. Pertaining to claim 13, Shoji in view of Johnson teach the circuit of claim 11 further comprising an ESC signal level detector connected to said ESC input, said ESC signal level

detector being configured to output a third signal when said first signal indicates an occurrence of the group consisting of said chucking spike, said de-chucking spike, and said arc event.

18. Pertaining to claim 14, Shoji in view of Johnson teach the circuit of claim 13 further comprising a gate having a first gate input, a second gate input, and a gate output, said first gate input being connected to said ESC signal level detector and said second gate input being connected to said VRF input, said gate being configured to output a fourth signal at said gate output when said third signal indicates an occurrence of said de-chucking spike and said arc event and not output said fourth signal when said third signal indicates an occurrence of said chucking spike.

19. Pertaining to claim 15, Shoji in view of Johnson teach the circuit of claim 11 further comprising a VRF signal level detector connected to said VRF input, said VRF signal level detector being configured to output a third signal when said second signal indicates that said plasma is activated.

20. Pertaining to claim 16, Shoji in view of Johnson teach the circuit of claim 15 further comprising a gate having a first gate input, a second gate input, and a gate output, said first gate input being connected to said ESC input and said second gate input receiving said third signal, said gate being configured to output a fourth signal at said gate output when said first signal indicates an occurrence of said de-chucking spike and said are event and not output said fourth signal when said first signal indicates an occurrence of said chucking spike.

21. Pertaining to claim 17, Shoji in view of Johnson teach the circuit of claim 11 further comprising a first gate having a first gate input, a second gate input, and a first gate output, said first gate input being connected to said ESC input and said second gate input being connected to said VRF input, said first gate being configured to output a third signal at said first gate output when said first signal indicates an occurrence of said de-chucking spike and said arc event and not output said third signal at said first gate output when said first signal indicates an occurrence of said chucking spike.

22. Pertaining to claim 18, Shoji in view of Johnson teach the circuit of claim 17 further comprising a power-on delay coupled between said VRF input and said second gate input, said power-on delay being configured to prevent said first gate from outputting said third signal at said first gate output during said occurrence of said chucking spike (see FIG 2 of Shoji which discloses a time delay of about 100 msec).

23. Pertaining to claim 19, Shoji in view of Johnson teach the circuit of claim 17 further comprising a second gate having a third gate input, a fourth gate input, and a second gate output, said third gate input being connected to said first gate output and said fourth gate input being connected to said VRF input, said second gate being configured to receive said third signal outputted by said first gate and output a fourth signal at said second gate during said occurrence of said de-chucking spike.

24. Pertaining to claim 20, Shoji in view of Johnson teach the circuit of claim 17 further comprising a power-off advance connected to said first gate output, said power-off advance being configured to prevent said arc detect output from indicating said occurrence of said de-chucking spike.

Conclusion

25. Any inquiry concerning this communication or earlier communications from the examiner should be directed to W. David Coleman whose telephone number is 571-272-1856. The examiner can normally be reached on Monday-Friday 9:00 AM - 5:30 PM.

26. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

27. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

W. David Coleman
Primary Examiner
Art Unit 2823

WDC